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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,766	09/05/2003	Jonathan Westphal	80006	6894

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,766	WESTPHAL, JONATHAN	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/655,766 filed on 9/5/2003. Claims 1-12 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Scholl et al., "BDD Minimization Using Symmetries," IEEE, Feb. 1999, pp. 81-100.

4. As to claims 1, 5, 8 and 11, Scholl et al. teach a method of designing logic circuits comprising representing multilevel logic schema in vector form (symmetric function can be represented in vector form); and for simplifying multilevel schema into a simplified form by exploiting symmetries (Fig. 3) in the logical schema (Boolean functions) (see page 81-3, section D page 84, paragraph III, starting page 84, paragraph IV, starting page 85). Scholl et al. teach detecting symmetries (partial) for both completely and incompletely specified Boolean functions before exploiting symmetries (page 82). Scholl et al. teach that logic function minimization comprises using symmetries by locating symmetrical variables side by side and receiving a modification of sifting: the symmetries sifting algorithm. The minimization would result minimizing the size of a logic function of the logic circuit design up to 70% (see abstract,

pages 81-82). Note that the Boolean functions are represented in vector form. The method must be operable on a computer system/computer network system having software stored thereon to execute the process. In order to produce a final product of logic circuit design, the logic circuit design must be synthesized and manufactured.

5. As to claims 2 and 7, School et al. teach simplifying multilevel logic schema comprising eliminating opposing couples. Scholl et al. teach detecting symmetries (partial) for both completely and incompletely specified Boolean functions before exploiting symmetries (page 82). Scholl et al. teach that logic function minimization comprises using symmetries by locating symmetrical variables side by side and receiving a modification of sifting: the symmetries sifting algorithm. The minimization would result minimizing the size of a logic function of the logic circuit design up to 70% (see abstract, pages 81-82).

6. As to claims 3, 9, 10 and 12 Scholl et al. teach a method of designing logic circuits comprising representing multilevel logic schema in vector form; and for simplifying multilevel schema into a simplified form by exploiting symmetries in the logical schema (see page 81-3, section D page 84, paragraph III, starting page 84, paragraph IV, starting page 85). Scholl et al. teach detecting symmetries (partial) for both completely and incompletely specified Boolean functions before exploiting symmetries (page 82). Scholl et al. teach that logic function minimization comprises using symmetries by locating symmetrical variables side by side and receiving a modification of sifting: the symmetries sifting algorithm. The minimization would result minimizing the size of a logic function of the logic circuit design up to 70% (see abstract,

pages 81-82). Note that the Boolean functions are represented in vector form. This would mean removing redundancy by eliminating opposing couples. In order to produce a final product of logic circuit design, the logic circuit design must be synthesized and manufactured.

7. As to claim 4, Scholl et al. teach detecting symmetries (partial) for both completely and incompletely specified Boolean functions before exploiting symmetries (page 82). Scholl et al. teach that logic function minimization comprises using symmetries by locating symmetrical variables side by side and receiving a modification of sifting: the symmetries sifting algorithm. The minimization would result minimizing the size of a logic function of the logic circuit design up to 70% (see abstract, pages 81-82). This would mean sliding symmetrical portions of the logic attached to opposing couples onto a point common to the opposing couples.

8. As to claim 6, Scholl et al. teach a method for designing logic circuits including minimizing logic functions (Boolean functions) by detecting symmetries (symmetric variables) and then exploiting the symmetries. The method must be executed on a computer system having software to communicate logical schema to one or more other computing devices inherently within the computer system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER